Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: JF201**

**APPROVED BY: DK DIE SIZE .031” X .032” DATE: 3/3/17**

**MFG: LINEAR SYSTEMS THICKNESS .009” P/N: LS845**

**DG 10.1.2**

#### Rev B, 7/19/02